**WHAT IS CLAIMED IS:**

1. A digital circuit comprising:

a digital processing component capable of operating at a plurality of selected clock frequencies, wherein a maximum delay time of a critical path in said digital processing component is determined by a level of a power supply, VDD, of said digital processing component;

an adjustable power supply capable of supplying VDD to said digital processing component; and

power supply adjustment circuitry that receives a first selected clock signal and adjusts said level of VDD such that said maximum delay time of said critical path is less than a pulse-width duration between a first clock edge of said first selected clock signal and a second clock edge of said first selected clock signal immediately following said first clock edge.

2. The digital circuit as set forth in Claim 1 wherein said power supply adjustment circuitry adjusts said level of VDD such that said maximum delay time is less than said pulse-width duration by not more than a maximum slack time threshold amount.

3. The digital circuit as set forth in Claim 2 wherein said power supply adjustment circuitry adjusts said level of VDD such that said maximum delay time is less than said pulse-width duration by not less than a minimum slack time threshold amount.

4. The digital circuit as set forth in Claim 3 wherein said power supply adjustment circuitry comprises clock generating circuitry capable of receiving an external reference clock signal and generating therefrom said first selected clock signal.

5. The digital circuit as set forth in Claim 4 wherein said power supply adjustment circuitry compares a frequency of said first selected clock signal to a frequency of a previous selected clock signal currently applied to said digital processing component and, in response to a determination that said first selected clock signal frequency is greater than said previous selected clock signal frequency, causes said clock generating circuitry to temporarily disable said first selected clock signal from being applied to said digital processing component.

6. The digital circuit as set forth in Claim 5 wherein said power supply adjustment circuitry causes said clock generating circuitry to apply said first selected clock signal to said digital processing component after said power supply adjustment circuitry adjusts said level of VDD such that said maximum delay time is less than said pulse-width duration by not more than a maximum slack time threshold amount and by not less than a minimum slack time threshold amount.

7. The digital circuit as set forth in Claim 5 wherein said power supply adjustment circuitry, in response to a determination that said first selected clock signal frequency is less than said previous selected clock signal frequency, causes said clock generating circuitry to apply said first selected clock signal to said digital processing component while said power supply adjustment circuitry adjusts said level of VDD such that said maximum delay time is less than said pulse-width duration by not more than a maximum slack time threshold amount and by not less than a minimum slack time threshold amount.

8. The digital circuit as set forth in Claim 7 wherein said power supply adjustment circuitry comprises N delay cells coupled in series, each of said N delay cells having a delay D determined by said level of VDD, wherein said first clock edge is applied to an input of a first delay cell and ripples sequentially through said N delay cells, and wherein said power supply adjustment circuitry: i) monitors outputs of at least a K delay cell and a K+1 delay cell, ii) determines that said first clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and iii) generates a control signal capable of adjusting VDD.

9. The digital circuit as set forth in Claim 8 wherein said power supply adjustment circuitry determines that said first clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when said second clock edge is applied to said first delay cell input.

10. The digital circuit as set forth in Claim 8 wherein a total delay from said first delay cell input to said K delay cell output is greater than said maximum delay time of said critical path.

11. The digital circuit as set forth in Claim 8 wherein said power supply adjustment circuitry increases VDD if said first clock edge has not reached said K delay cell output.

12. The digital circuit as set forth in Claim 8 wherein said power supply adjustment circuitry decreases VDD if said first clock edge has reached said K+1 delay cell output.

13. A method of operating a digital circuit for adjusting a power supply level, VDD, of a digital processing component capable of operating at a plurality of selected clock frequencies, wherein a maximum delay time of a critical path in the digital processing component is determined by a level of a power supply, VDD, of the digital processing component, the method of operating the digital circuit comprising the steps of:

supplying VDD to the digital processing component from an adjustable power supply;

receiving a first selected clock signal; and

adjusting the level of VDD such that the maximum delay time of the critical path is less than a pulse-width duration between a first clock edge of the first selected clock signal and a second clock edge of the first selected clock signal immediately following the first clock edge.

14. The method as set forth in Claim 13 wherein the step of adjusting comprises the sub-step of adjusting the level of VDD such that the maximum delay time is less than the pulse-width duration by not more than a maximum slack time threshold amount.

15. The method as set forth in Claim 14 wherein the step of adjusting comprises the sub-step of adjusting the level of VDD such that the maximum delay time is less than the pulse-width duration by not less than a minimum slack time threshold amount.

16. The method as set forth in Claim 15 wherein the step of receiving the first selected clock signal comprises the sub-step of receiving an external reference clock signal and generating therefrom the first selected clock signal.

17. The method as set forth in Claim 16 further comprising the steps of:

comparing a frequency of the first selected clock signal to a frequency of a previous selected clock signal currently applied to the digital processing component; and

in response to a determination that the first selected clock signal frequency is greater than the previous selected clock signal frequency, temporarily disabling the first selected clock signal from being applied to the digital processing component.

18. The method as set forth in Claim 17 further comprising the step of applying the first selected clock signal to the digital processing component after the power supply adjustment circuitry adjusts the level of VDD such that the maximum delay time is less than the pulse-width duration by not more than a maximum slack time threshold amount and by not less than a minimum slack time threshold amount.

19. The method as set forth in Claim 17 further comprising the step, in response to a determination that the first selected clock signal frequency is less than the previous selected clock signal frequency, of apply the first selected clock signal to the digital processing component while the power supply adjustment circuitry adjusts the level of VDD such that the maximum delay time is less than the pulse-width duration by not more than a maximum slack time threshold amount and by not less than a minimum slack time threshold amount.

20. The method as set forth in Claim 19 wherein the digital circuit comprises a power supply adjustment circuitry comprising N delay cells coupled in series, each of the N delay cells having a delay D determined by the level of VDD, wherein the first clock edge is applied to an input of a first delay cell and ripples sequentially through the N delay cells, and wherein the method further comprises the steps of:

monitoring outputs of at least a K delay cell and a K+1 delay cell;

determining that the first clock edge has reached an output of the K delay cell and has not reached an output of the K+1 delay cell; and

generating a control signal capable of adjusting VDD.

21. The method as set forth in Claim 20 further comprising the step of determining that the first clock edge has reached the K delay cell output and has not reached the K+1 delay cell output when the second clock edge is applied to the first delay cell input.

22. The method as set forth in Claim 20 wherein a total delay from the first delay cell input to the K delay cell output is greater than the maximum delay time of the critical path.

23. The method as set forth in Claim 20 further comprising the step of increasing VDD if the first clock edge has not reached the K delay cell output.

24. The method as set forth in Claim 20 further comprising the step of decreasing VDD if the first clock edge has reached the K+1 delay cell output.